Experimental verification of the usefulness of the nth power law MOSFET model under hot carrier wearout

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Abstract

In this paper the usefulness of the *n*th power law MOSFET model under Hot Carrier Injection (HCI) wearout has been experimentally demonstrated. In order to do that, three types of nFET transistors have been analyzed under different HCI conditions and the *n*th power law MOSFET model has been extracted for each sample. The results show that the model can reproduce the MOSFET behavior under HCI wearout mechanism. Therefore, the impact of HCI on circuits can be analyzed by using the *n*th power law MOSFET model.

1. Introduction

The *n*th power law MOSFET model, also namely Sakurai–Newton model, is a well-known analytical model, which can reproduce the MOSFET behavior with only six parameters [1]. The model is expressed in the following equation:

$V_{DSAT}=K\cdot(V_{GS}-V_{TH})^{m}$

$I_{DSAT}=B\cdot(V_{GS}-V_{TH})^{n}$

$$\begin{cases} V_{GS} < V_{TH} & I_D = 0\,\mathrm{A} \\ V_{GS} \geq V_{TH} \begin{cases} V_{DS} < V_{DSAT} & I_D = I_{DSAT}\cdot(1+\lambda_a\cdot V_{DS})\cdot\left(2-\frac{V_{DS}}{V_{DSAT}}\right)\cdot\frac{V_{DS}}{V_{DSAT}} \\ V_{DS} \geq V_{DSAT} & I_D = I_{DSAT}\cdot(1+\lambda_a\cdot V_{DS}) \end{cases} \end{cases} \quad (1)$$

where V_{GS} and V_{DS} are the gate-to-source and the drain-to-source voltages, respectively. V_{TH} denotes the threshold voltage, V_{DSAT} the drain saturation voltage and I_{DSAT} the drain saturation current. Parameters K and m control the linear region characteristics whereas B and n determine the saturated region characteristics. λ is related to the finite drain conductance in the saturated region. The simplicity of the model allows an analytical processing. The model (or models derived from it) has been extensively used in order to evaluate the behavior of several CMOS circuits [1], [2], [3] and [4] due to its simplicity. It should be pointed out that the *n*th power law MOSFET parameters correspond to an analytical non-physical model and it is only valid for voltage gates above the voltage threshold.

Hot Carriers Injection (HCI) is the phenomenon in solid-state or semiconductor electronic devices where either an electron or a “hole” gains sufficient kinetic energy to overcome a potential barrier necessary to break an interface state [5]. HCI does not always lead to circuit failure [6], but provokes undesired effects such as the reduction of the speed at which the transistor can operate. Therefore, to determine how sensitive are the electronic circuits to HCI, some accurate models are required. In this sense, MOSFET models, which take into account the effects of HCI, and that could be implemented in circuit simulators are required. Equivalent electrical circuits for FETs under HCI have been already presented, which can be included in SPICE simulators. In this approach, additional components are needed [7]. An alternative approach is the description of the HCI MOSFET using models like, for example, BSIM, whose parameters are extracted after the HCI stress. This approach would be the most accurate, but a large number of parameters and a complex extraction process are required. In this work, and alternative approach has been followed, and the usefulness of *n*th power law MOSFET model under HCI effect has been demonstrated experimentally. Moreover, the impact of HCI wearout on each Sakurai–Newton model parameters has been experimentally obtained.

2. Experimental

To analyze the impact of the HCI in the nMOS, a Keithley 2602A Source-meter, a digital multimeter and an acquisition board have been used, all of them controlled with a laptop (Fig. 1). First of all, it is necessary to obtain the stress conditions. The V_{DS} stress voltage (V_{STRESS}) should be equal to the drain-to-source voltage breakdown minus 0.5 V. The V_{GS} stress voltage is obtained by measuring the substrate current (I_{SUB}) whereas the V_{GS} is swept with the V_{DS} set to V_{STRESS}. The V_{GS} stress voltage is defined as the gate voltage corresponding to the maximum I_{SUB} value on the I_{SUB}–V_{GS} curve. Table 1 summarizes the different stress voltages applied to the different type of nMOS transistors.

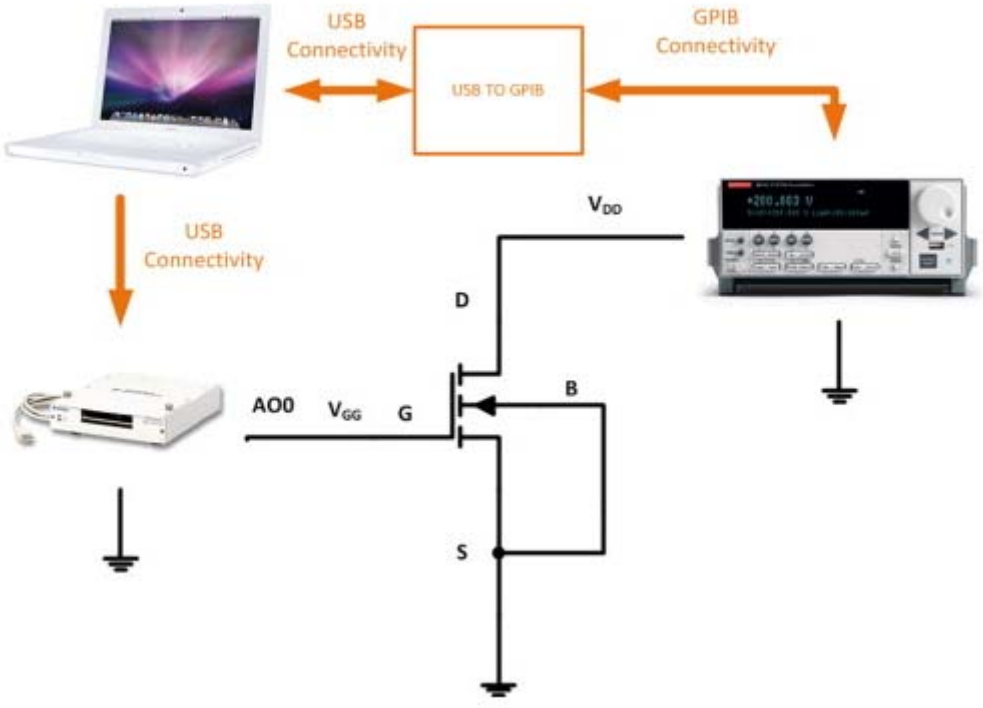

Fig. 1. Set-up to obtain the impact of the HCI on nMOS.

Table 1. Type of transistor measured and stress voltages applied.

	$V_{DS}\|_{STRESS}$ (V)	$V_{GS}\|_{STRESS}$ (V)
High voltage long (W = 10 μm L = 1.52 μm)	7	2.6
	5	1.9
High voltage short (W = 10 μm L = 0.38 μm)	7	2.05
	5	1.6
Low voltage long (W = 10 μm L = 0.4 μm)	3	0.97
	2.5	0.9

3. Results

Fig. 2 and Fig. 3 show the ID–VDS and the ID–VGS curve characteristic, respectively, for several stress time. As it is observed, the drain saturation current is reduced due to the effect of the HCI. Fig. 4 and Fig. 5 plot the fitting of the measurements and the Sakurai–Newton MOSFET model for the fresh component and after 700 s of stress. A good correlation between the mathematical model and the measurements has been obtained. Therefore, the impact of HCI wearout on each *n*th power law MOSFET model has been evaluated and it is shown below.

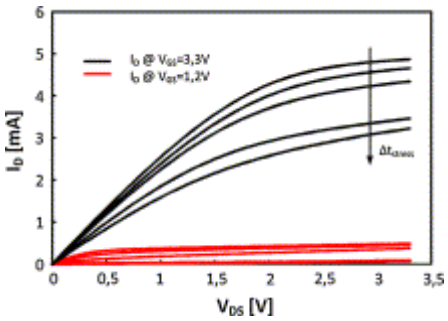

Fig. 2. I_D–V_{DS} for several stress time and several V_{GS}.

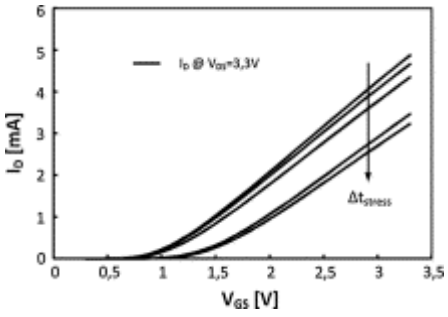

Fig. 3. I_D–V_{GS} for several stress time.

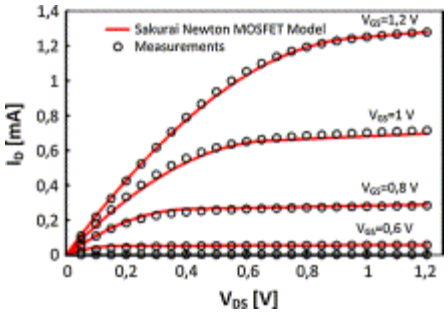

Fig. 4. Comparison between the measurements and the Sakurai–Newton MOSFET model for the fresh component.

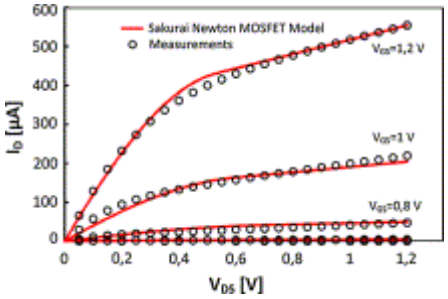

Fig. 5. Comparison between the measurements and the Sakurai–Newton MOSFET model for the t_{STRESS} = 700 s.

Fig. 6 depicts the increase of the finite drain conductance (λ), which produces a change in the slope of the drain current (in the saturated region), as can be observed in Fig. 2. Fig. 7 plots the threshold voltage shift, which is more significant on the high voltage short transistor, rather than on the high voltage long and low voltage long. The VTH enhancement provokes a drain current decrease, as can be observed on Fig. 3. The n parameters shift is plotted in Fig. 8, which corresponds to a value less than 10% for the three types of nMOS transistors. On the other hand, B parameter shift is plotted in Fig. 9, which decreases as long as the stress time increases. This parameter is related with the transconductance of the device. Fig. 10 and Fig. 11 show the K and m parameters shift, related with control of the linear region. Both parameters are modified due to the change of the linear ID–VDS curve characteristic, as seen in Fig. 4 and Fig. 5.

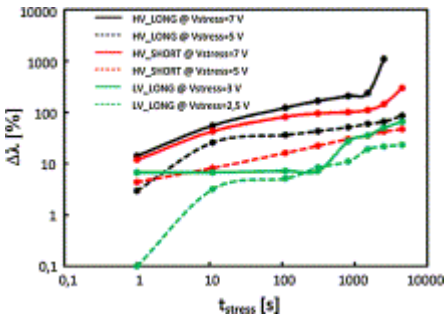

Fig. 6. Variation of the finite drain conductance (*λ*) versus the stress time.

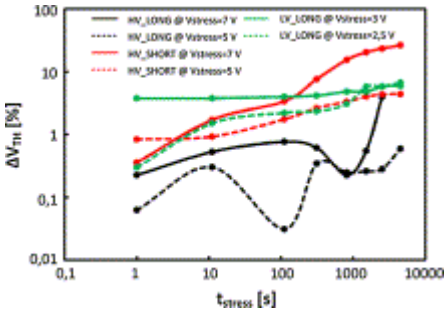

Fig. 7. Variation of the threshold voltage versus the stress time.

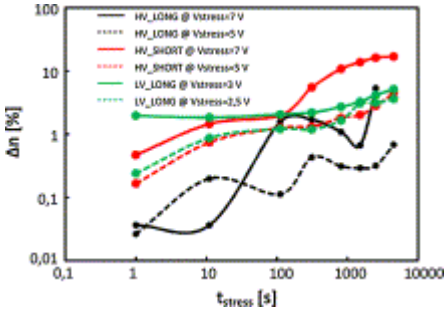

Fig. 8. Variation of the *n* parameter versus the stress time.

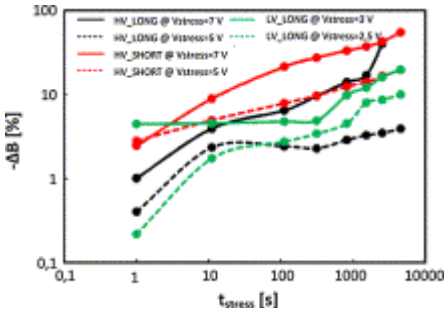

Fig. 9. Variation of the transconductance (*B*) versus the stress time.

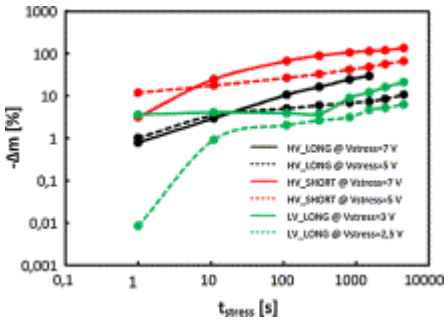

Fig. 10. Variation of the *m* parameter versus the stress time.

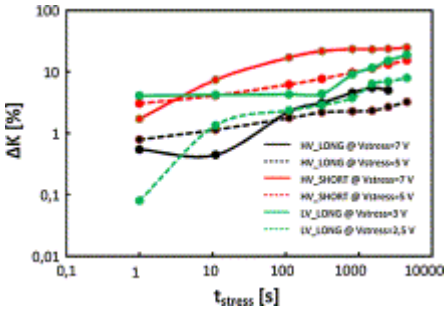

Fig. 11. Variation of the *K* parameter versus the stress time.

4. Conclusions

In this paper, the usefulness of the Sakurai–Newton MOSFET model under HCI wearout has been experimentally demonstrated for different nFET transistors and different stress conditions. The impact of HCI on each parameter has been also analyzed. The results show that the models can be useful in order to fit the MOSFET behavior under HCI stress and it can be included in a circuit simulator to predict the impact of HCI on digital circuit behavior, where the sub-threshold behaviors are not so important.

Acknowledgements

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